CLAIMS

What is claimed is:

1. A latch circuit for complementary dynamic logic, said latch circuit comprising:

a first logic gate having a first input and a second input, wherein said first input is connected to a first precharged internal node of said complementary dynamic logic, and said second input is connected to a first differential output of said complementary dynamic logic;

a second logic gate having a first input and a second input, wherein said first input is connected to a second precharged internal node of said complementary dynamic logic, and said second input is connected to a second differential output of said complementary dynamic logic;

a third logic gate having a first input connected to an output of said first logic gate to provide a first output for said latch circuit; and

a fourth logic gate having a first input connected to an output of said second logic gate to provide a second output for said latch circuit, wherein said second output is connected to a second input of said third logic gate, and said first output is connected to a second input of said fourth logic gate.

2. The latch circuit of Claim 1, wherein said first and second outputs are differential outputs.

3. The latch circuit of Claim 1, wherein inputs of said first and second logic gates are connected to transistors at the top of the stack of transistors within said first and second logic gates.

4. A latch circuit capable of ensuring race-free staging of signals for a dynamic logic circuit, said latch circuit comprising:

a first NAND gate having a first input and a second input, wherein said first input is connected to a first precharged internal node of said complementary dynamic logic, and said second input is connected to a first differential output of said complementary dynamic logic;

a second NAND gate having a first input and a second input, wherein said first input is connected to a second precharged internal node of said complementary dynamic logic, and said second input is connected to a second differential output of said complementary dynamic logic;

a third NAND gate having a first input connected to an output of said first NAND gate to provide a first output for said latch circuit; and

a fourth NAND gate having a first input connected to an output of said second NAND gate to provide a second output for said latch circuit, wherein said second output is connected to a second input of said third NAND gate, and said first output is connected to a second input of said fourth NAND gate.

5. The latch circuit of Claim 1, wherein said first and second outputs are differential outputs.

6. The latch circuit of Claim 1, wherein inputs of said first and second NAND gates are connected to transistors at the top of the stack of transistors within said first and second NAND gates.

7. A latch circuit capable of ensuring race-free staging of signals for a dynamic logic circuit, said latch circuit comprising:

a first NOR gate having a first input and a second input, wherein said first input is connected to a first precharged internal node of said complementary dynamic logic, and said second input is connected to a first differential output of said complementary dynamic logic;

a second NOR gate having a first input and a second input, wherein said first input is connected to a second precharged internal node of said complementary dynamic logic, and said second input is connected to a second differential output of said complementary dynamic logic;

a third NOR gate having a first input connected to an output of said first NOR gate to provide a first output for said latch circuit; and

a fourth NOR gate having a first input connected to an output of said second NOR gate to provide a second output for said latch circuit, wherein said second output is connected to a second input of said third NOR gate, and said first output is connected to a second input of said fourth NOR gate.

8. The latch circuit of Claim 1, wherein said first and second outputs are differential outputs.

9. The latch circuit of Claim 1, wherein inputs of said first and second NOR gates are connected to transistors at the top of the stack of transistors within said first and second NOR gates.